UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,097	05/30/2006	Mitsuru Ueda	36856.1440	1870

54066 7590 11/27/2009

MURATA MANUFACTURING COMPANY, LTD.
C/O KEATING & BENNETT, LLP
1800 Alexander Bell Drive
SUITE 200
Reston, VA 20191

EXAMINER	
CHEN, XIAOLIANG	
ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
11/27/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JKEATING@KBIPLAW.COM
uspto@kbiplaw.com
cbennett@kbiplaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/596,097	UEDA ET AL.	
	Examiner	Art Unit	
	Xiaoliang Chen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgement is made of Amendment filed 11-10-09.

2. Claims 8, 9, 14, 15 and 19 are amended.

3. Claims 1-7 are canceled.

4. Claim 21 is added.

Response to Arguments

5. Since Claims 9, 15 and 19 are amended, the claim rejections of Claims 9, 15 and 19 under 35 U.S.C. 112, second paragraph, have been withdrawn.

6. Applicant's arguments with respect to claims 8 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

7. Claim 21 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

The new added Claim 21 is as the same as Claim 17.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 8-10 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai (US20010026435) in view of Alcoe (US7087846).

Re Claim 8, Sakai show and disclose

A laminated ceramic electronic component comprising:

a plurality of ceramic sheets (the ceramic green sheets are laminated together [0017]), each including an internal conductor pattern (26, fig. 2) having a first land (29, fig. 1) at one end of the internal conductor pattern (at left end portion of 26, fig. 2) and a second land (29, fig. 1) at the other end (right end

portion of 26, fig. 2) of the internal conductor pattern and having a via hole (via hole of 25, fig. 2) provided therein, the plurality of ceramic sheets being laminated to define a laminate (the ceramic green sheets are laminated together [0017]); wherein

the via hole is filled with a conductive material (the conductive paste is filled into the through-hole [0025]);

the internal conductor patterns disposed on different ones of the plurality of ceramic sheets (fig. 2) are electrically connected to each other through the via hole (fig. 2);

the first land is arranged so as to cover the via hole (fig. 2) and the first land provided in one of the plurality of ceramic sheets is electrically connected to the second land provided in another of the plurality of ceramic sheets through the via hole provided in the one ceramic sheet (the connecting land is positioned at an end of the line conductor, i.e., the end of the line conductor is connected to the via-hole conductor [0037]);

an area of the via hole is less than area of the first land and an area of the second land (connecting land having a diameter greater than the diameter of the via-hole conductor [ABSTRACT]);

Sakai does not disclose

the area of the second land is larger than the area of the first land.

Alcoe teaches a device wherein

the area of the second land (25, fig 1-1A) is larger than the area of the first land (29, fig. 1-1A).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a larger second land for a conductor as taught by Alcoe in the electronic device of Sakai, in order to connect to larger size via hole, and in order to be able to allow slight variations in alignment of the via with the land when the layers laminated together.

Re Claim 9, Sakai show and disclose

The laminated ceramic electronic component according to Claim 8, wherein the second land extends from a projection plane of the first land to a projection plane of the internal conductor pattern (both lands projected from two ends of 26 the internal conductor pattern, fig. 1-2);

Re Claim 10, Sakai and Alcoe disclose

The laminated ceramic electronic component according to Claim 8, wherein the area of the second land is about 1.10 to about 2.25 times as wide as the area of the first land (fig. 2, Alcoe).

Re Claim 14, Sakai show and disclose

A manufacturing method for a laminated ceramic electronic component, comprising the steps of:

printing an internal conductor pattern (26, fig. 2, by printing, a line conductor is formed [0016]) having a first land (29, fig. 1) at one end of the internal conductor pattern (at left end portion of 26, fig. 2) and a second land (29,

fig. 1) at the other end of the internal conductor pattern (right end portion of 26, fig. 2) on the surface of a ceramic sheet (the ceramic green sheets [0017]) having a hole (hole for 25, fig. 1) for a via hole (via hole 25, fig 2) formed therein by using a conductive material (the conductive paste is filled into the through-hole [0025]) such that the first land covers the hole for via hole;

filling the conductive material in the hole for the via hole (the conductive paste is filled into the through-hole [0025]); and laminating a plurality of ceramic sheets (the ceramic green sheets are laminated together [0017]) such that the first land in one of the plurality of ceramic sheets is electrically connected to the second land in another of the plurality of ceramic sheets through the via hole formed in the one of the plurality of ceramic sheets (the connecting land is positioned at an end of the line conductor, i.e., the end of the line conductor is connected to the via-hole conductor [0037]) to obtain a laminate (the ceramic green sheets are laminated together [0017]);

an area of the via hole is less than area of the first land and an area of the second land (connecting land having a diameter greater than the diameter of the via-hole conductor [ABSTRACT]);

Sakai does not disclose

the area of the second land is larger than the area of the first land.

Alcoe teaches a device wherein

the area of the second land (25, fig 1-1A) is larger than the area of the first land (29, fig. 1-1A).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a larger second land for a conductor as taught by Alcoe in the electronic device of Sakai, in order to connect to larger size via hole, and in order to be able to allow slight variations in alignment of the via with the land when the layers laminated together.

Re Claim 15, Sakai show and disclose

The manufacturing method for a laminated ceramic electronic component according to Claim 14, wherein the second land extends from a projection plane of the first land to a projection plane of the internal conductor pattern (both lands projected from two ends of 26 the internal conductor pattern, fig. 1-2);

Re Claim 16, Sakai and Alcoe disclose

The manufacturing method for a laminated ceramic electronic component according to Claim 14, wherein the area of the second land is about 1.10 to about 2.25 times as wide as the area of the first land (fig. 2, Alcoe).

11. Claims 11-13 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of Alcoe as applied to claims 8 and 14 above, further in view of Maeda et al. (US20050122699).

Re Claim 11, Sakai and Alcoe disclose

The laminated ceramic electronic component according to Claim 8, Sakai and Alcoe do not disclose

wherein the internal conductors included on the plurality of ceramic sheets define a spiral coil.

Maeda et al. teaches a device wherein

the internal conductors included on the plurality of ceramic sheets define a spiral coil (spiral coil [0042]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the spiral coil conductor pattern as taught by Maeda et al. in the electronic device of Sakai, in order to form and define the shape of a spiral coil conductor inside the laminate (Maeda et al., Para. [0072]).

Re Claim 12, Sakai show and disclose

The laminated ceramic electronic component according to Claim 11, wherein terminal ends of the spiral coil define lead-out electrodes (27, fig. 2).

Re Claim 13, Sakai and Alcoe disclose

The laminated ceramic electronic component according to Claim 11, Sakai and Alcoe do not disclose

two additional ceramic sheets which do not include any internal conductors disposed therein, one of the two additional ceramic sheets being disposed on an upper surface of the laminate, and the other of the two additional ceramic sheets being disposed on a lower surface of the laminate.

Maeda et al. teaches a device wherein

two additional ceramic sheets (top and bottom sheets, fig. 2) which do not include any internal conductors disposed therein (fig. 20, one of the two additional ceramic sheets being disposed on an upper surface of the laminate

(fig. 2), and the other of the two additional ceramic sheets being disposed on a lower surface of the laminate (fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the additional ceramic sheets as taught by Maeda et al. in the electronic device of Sakai, in order to provide the external extension electrodes for the spiral coil conductor of laminated electronic device (Maeda et al., Para. [0005]).

Re Claim 18, Sakai and Alcoe disclose

The manufacturing method for a laminated ceramic electronic component according to Claim 14,

Sakai and Alcoe do not disclose

arranging the internal conductors on the plurality of ceramic sheets so as to define a spiral coil.

Maeda et al. teaches a device wherein

arranging the internal conductors on the plurality of ceramic sheets so as to define a spiral coil (spiral coil [0042]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the spiral coil conductor pattern as taught by Maeda et al. in the electronic device of Sakai, in order to form and define the shape of a spiral coil conductor inside the laminate (Maeda et al., Para. [0072]).

Re Claim 19, Sakai show and disclose

The manufacturing method for a laminated ceramic electronic component according to Claim 18, wherein terminal ends of the spiral coil define lead-out electrodes (27 fig. 2);

Re Claim 20, Sakai and Alcoe disclose

The manufacturing method for a laminated ceramic electronic component according to Claim 14,

Sakai and Alcoe do not disclose

providing two additional ceramic sheets which do not include any internal conductors printed therein; disposing one of the two additional ceramic sheets on an upper surface of the laminate; and disposing the other of the two additional ceramic sheets on a lower surface of the laminate.

Maeda et al. teaches a device wherein

providing two additional ceramic sheets (top and bottom sheets, fig. 2) which do not include any internal conductors printed therein (fig. 2); disposing one of the two additional ceramic sheets on an upper surface of the laminate (fig. 20; and disposing the other of the two additional ceramic sheets on a lower surface of the laminate (fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the additional ceramic sheets as taught by Maeda et al. in the electronic device of Sakai, in order to provide the external extension electrodes for the spiral coil conductor of laminated electronic device (Maeda et al., Para. [0005]).

12. Claims 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of Alcoe as applied to claim 14 above, further in view of Niwa et al. (US4237606).

Re Claims 17 and 21, Sakai and Alcoe disclose

The manufacturing method for a laminated ceramic electronic component according to Claim 14,

wherein the internal conductor pattern is printed (26, fig. 2, by printing, a line conductor is formed [0016]) on a ceramic sheet having the hole (hole of 25, fig. 1) for a via hole (via hole of 25, fig 2) formed therein and the hole for the via hole is filled with a conductive material (the conductive paste is filled into the through-hole [0025]),

Sakai and Alcoe do not disclose

the printing and filling without providing a carrier film on a back surface of the ceramic sheet.

Niwa et al. teaches a device wherein

the printing (a pattern is printed on the green sheet according to a wiring pattern [col. 1, line 38]) and filling (the hole is filled with the electrically conductive paste [col. 1, line 43]) without providing a carrier film on a back surface of the ceramic sheet.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the printing and filling method as

taught by Niwa et al. in the electronic device of Sakai, in order to simplify the printing and filling processes and reduce the cost of the electronic device.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US-20020052065 US-20020089050 US-20060001149 US-3781596 US-4036550 US-4535312 US-4591411 US-6441493 US-6815837.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiaoliang Chen whose telephone number is (571)272-9079. The examiner can normally be reached on 8:00-5:00 (EST), Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jinhee J Lee/
Supervisory Patent Examiner, Art Unit 2841

Xiaoliang Chen
Examiner
Art Unit 2841